J Electroceram (2007) 19:357–362
DOI 10.1007/s10832-007-9036-3

Taking piezoelectric microsystems from the laboratory to production

H. Ræder · F. Tyholdt · W. Booij · F. Calame · N. P. Østbø · R. Bredesen · K. Prume · G. Rijnders · P. Muralt

Received: 19 March 2006 / Accepted: 8 September 2006 / Published online: 6 March 2007

Abstract Reliable integration of piezoelectric thin films into silicon-based microsystems on an industrial scale is a key enabling technology for a wide range of future products. However, current knowledge in the field is mostly limited to the conditions and scale of academic laboratories. Thus, knowledge on performance, reliability and reproducibility of the films and methods at industrial level is scarce. The present study intends to contribute to the development of reliable technology for integration of piezoelectric thin films into MEMS on an industrial scale. A test wafer design that contained more than 500 multimorph cantilevers, bridges and membranes in the size range between 50 and 1,500 μm was developed. The active piezoelectric material was a ~2 μm thin film of lead zirconate titanate (PZT) deposited by a state-of-the-art chemical solution deposition (CSD) procedure. Automated measurements of C(V) and dielectric dissipation factor at 1 kHz were made on more than 200 devices at various locations across the wafer surface. The obtained standard deviations were 4.5 and 11% for the permittivity and dissipation factor, respectively. Values for the transverse piezoelectric charge coefficient, $e_{31,f}$, of up to −15.1 C/m^2 were observed. Fatigue tests with a 5 kHz signal applied to a typical cantilever at ± 25 V led to less than 10% reduction of the remanent polarisation after 2 × 10^7 bipolar cycles. Cantilever out-of-plane deflection at zero field measured after poling was less than 1.1% for a typical 800 μm cantilever.

Keywords Piezoelectric · Piezoceramics · Microsystems · MEMS · Thin film · Production

H. Ræder (✉) · F. Tyholdt · W. Booij · N. P. Østbø · R. Bredesen
SINTEF,
P. O. Box 124, Blindern,
0314 Oslo, Norway
e-mail: Henrik.Raeder@sintef.no

F. Calame · P. Muralt
EPFL-LC, MXD Ecublens,
1015 Lausanne, Switzerland

K. Prume
aixACCT Systems GmbH,
Dennewartstrasse 25,
52068 Aachen, Germany

G. Rijnders
University of Twente,
P.O. Box 217, 7500 AE Enschede, The Netherlands

1 Introduction

Since the early 1990s, piezoelectric thin films of various types have been studied intensively in academic institutions, and improved methods to prepare them have been developed at laboratory scale. At the same time, many laboratories and small companies—both existing and newly established ones—have come up with innovative ideas for new types of sensors, actuators and other products based on silicon MEMS (micro-electromechanical systems) technology that incorporates such films as main functional elements [reviewed in 7]. Examples of such devices are; ultrasonic imaging transducers, pressure and flow sensors, accelerometers, acoustic wave devices, micromotors, micropumps, and microsensors for chemical analysis. Reliable technology for integration of piezoelectric thin films into MEMS on an industrial scale is a key tool to realise these new products.

Established techniques for mechanical actuation/sensing in MEMS often cannot fulfil the combined requirements of

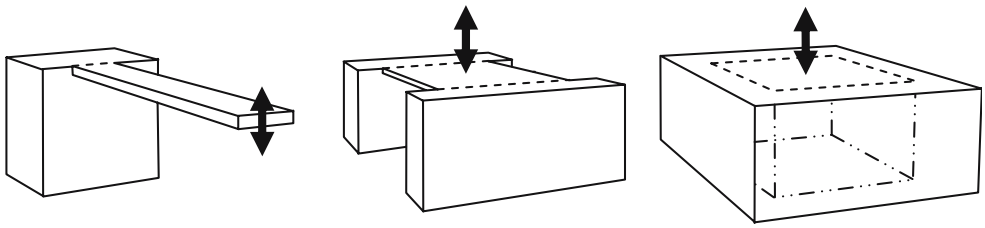

Fig. 1 Basic designs of piezoelectric multimorph actuators, utilizing the transverse piezoelectric effect; (*from left*) cantilever, bridge and fixed membrane

force, speed and energy efficiency, making the practical realisation of new concepts impossible or non-competitive. The most common mechanisms are based on the electrostatic, piezoresistive and thermal effect. Thermal actuation is generally slow and the amplitude is small, the piezoresistive effect can be used for sensing only, and electrostatic actuation is non-linear and has mechanical drawbacks. It is clear that piezoelectric thin film elements on silicon can fill this gap. The reliable integration of piezoelectric thin films into MEMS on an industrial scale is therefore a key enabling technology for a wide range of future products. However, current knowledge in the field is mostly limited to the conditions and scale of academic laboratories and knowledge on performance, reliability and reproducibility of the films and methods at industrial level is scarce. The present study intends to contribute to the development of reliable technology for integration of piezoelectric thin films into MEMS on an industrial scale.

The most commonly employed configuration of piezoelectric thin film elements in Si-based MEMS is to integrate it as one of several layers of different materials in a multimorph or heteromorph structure. The film is sandwiched between thin metal electrodes (usually Cr/Au and Pt) and the three layers are fixed to a single-crystal silicon wafer through an adhesion layer (usually TiO_2/Ti). When a voltage or an oscillating signal is applied between the electrodes, the film changes dimensions both in the direction normal to the film plane (thickness mode) and in the plane parallel to the film (transverse mode). The thickness mode linear movement is small, only a few nm for a μm-thick film. To obtain larger deflections and better impedance matching in acoustic systems, the transverse effect is commonly utilized. If an alternating voltage is applied to the film it will expand and contract according to the electric field in the plane parallel to the film and the multimorph will hence vibrate in one of several bending modes. The system can be designed in several ways, but most relevant designs can be categorised into the three main groups shown in Fig. 1; *cantilever*, *bridge* and *fixed membrane*.

The first commercial piezoelectric MEMS devices will likely be for small-scale applications where only a few thousand devices are made. Since several hundred devices

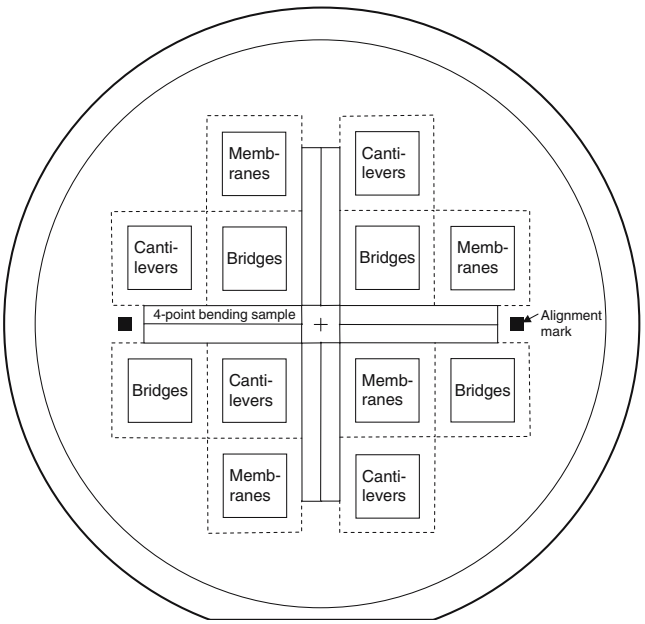

Fig. 2 Schematic design layout of the test wafers

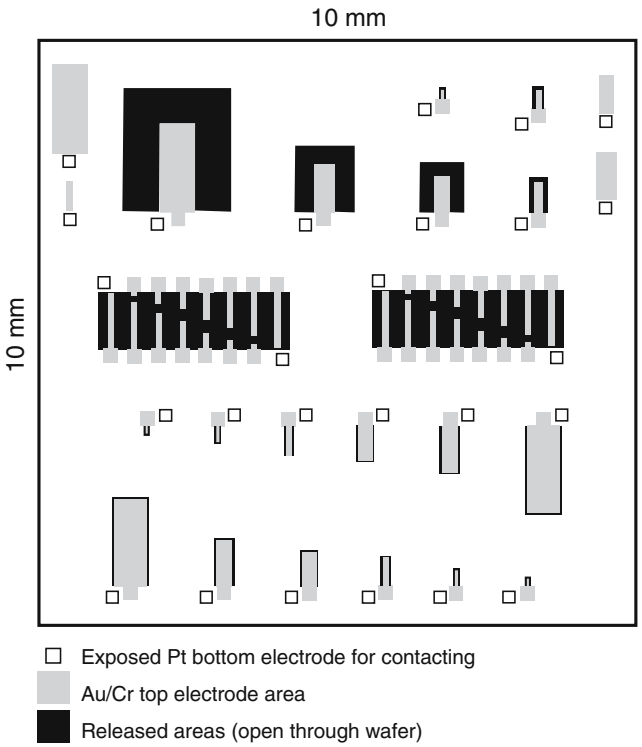

Fig. 3 Schematic design layout of a 10×10 mm square dedicated to cantilevers. Designs with both narrow (5 and 10 μm) and wide (equal to cantilever width) open rims were included

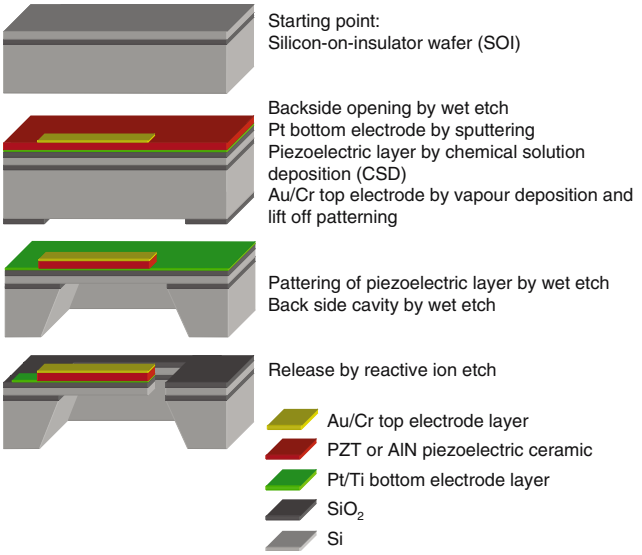

Fig. 4 Main processing steps for the multimorph cantilevers

can be processed in parallel on a single wafer, such production can be made in research labs if industrially qualified procedures are available. While a very low yield is acceptable for academic research (most devices can be discarded), a high yield is required for small-scale production to keep costs low. One objective of this study has therefore been to investigate the uniformity of device characteristics and performance over a full wafer. The methods that were used to prepare the devices were standard Si-MEMS processing steps combined with state-of-the-art PZT thin film preparation methods developed by the authors and reported in literature [6, 9].

A special test wafer design was developed that contained more than 500 devices of various sizes in the three design

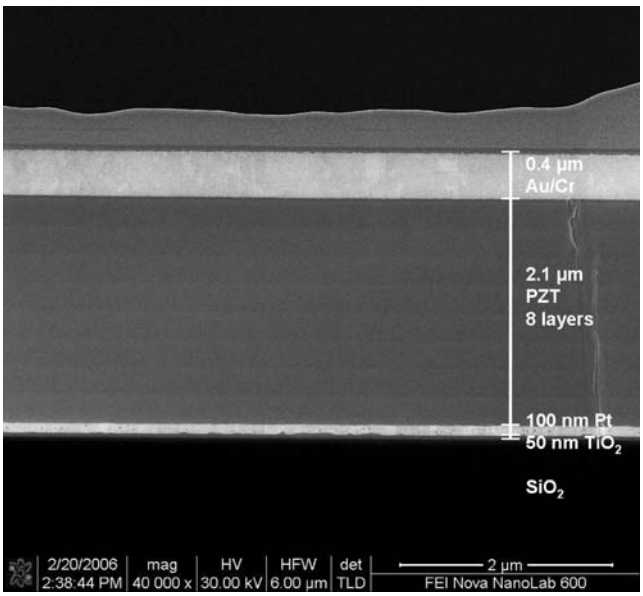

Fig. 5 SEM micrograph of a multimorph cross section milled by focused ion beam

Table 1 Transverse piezoelectric charge coefficients measured at three frequencies.

Frequency [Hz]	$e_{31,f}$ [C/m^2]
0.1	−15.1
1	−14.4
10	−14.1

categories shown in Fig. 1. This paper reports the design and preparation of the test wafer and the results obtained from wafer-level testing and characterisation.

2 Experimental procedure

2.1 Design

The test wafer design was based on the use of 100 mm diameter silicon-on-insulator (SOI) <100> oriented silicon wafers (IBIS Technology Corp., MA, USA). The basic design elements were grouped into twelve 10×10 mm squares surrounded by 2.5 mm wide frames. The purpose of the frames was to facilitate handling, mounting and packaging of the squares after dicing. The design also included eight special samples intended for 4-point bending tests for measuring the effective transverse piezoelectric effect, $e_{31,f}$. A schematic overview of the design layout is shown in Fig. 2. The design layout of a 10×10 mm square dedicated to cantilevers is shown in Fig. 3.

Each of the squares was dedicated to either cantilevers, bridges or fixed membranes. The length dimension of the device elements varied from 50 to 1,500 µm.

It is well known that all layers except SiO_2 induce tensile stresses in multimorph structures of this type, as described in [5]. By adjusting the thermal oxide thickness so that its compressive stress cancels out the stresses in the remaining structure one can avoid bending of the cantilevers. Analytical modelling of stress levels in the structures were carried out to calculate the optimal oxide thickness. Details are reported in a separate publication [1].

Table 2 Average values and standard deviations for relative permittivity and dissipation factor measured at 0 V and 1 kHz for more than 200 devices.

	Average value	Standard deviation
Relative dielectric permittivity, ε_r	1,130	51 (4.5%)
Dielectric dissipation factor, tanδ	0.029	0.0032 (11%)

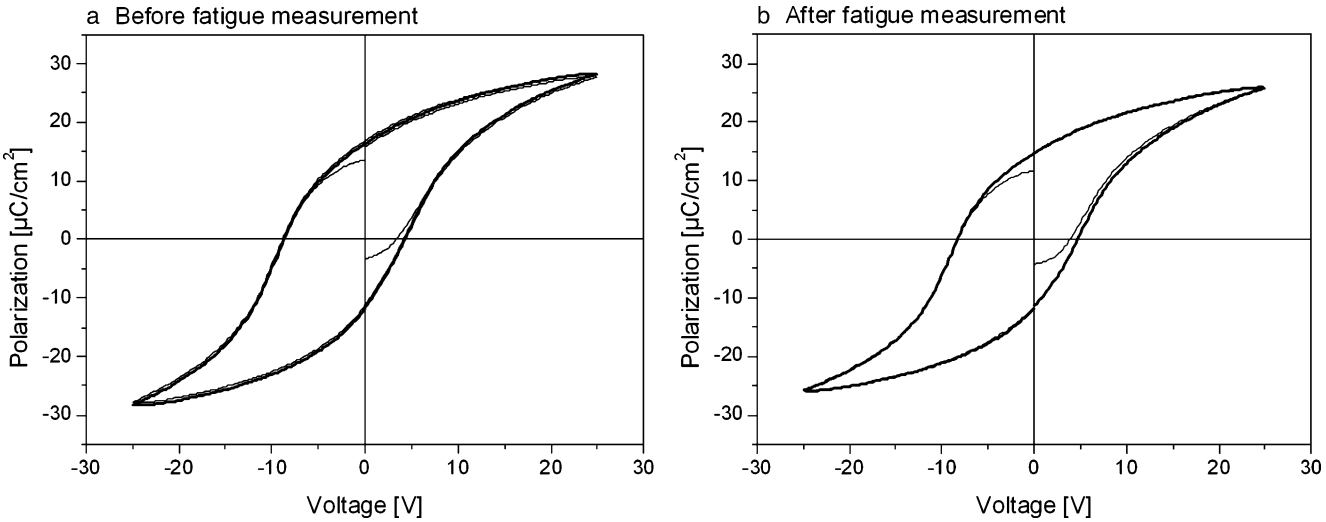

Fig. 6 Polarisation hysteresis loops recorded before (**a**) and after (**b**) fatigue test. The size of the cantilever was 300×60 µm. The curves were recorded using a TF 2000 ferroelectric analyser (aixACCT Systems GmbH, Germany)

2.2 Preparation

The devices were prepared through a series of processing steps as illustrated in Fig. 4.

The SOI wafer was first thermally oxidised to obtain an oxide thickness of 1.3 µm. The backside oxide was then opened using a lithographic mask and wet etching by HF. On the front side, a thin TiO_2/Ti layer was deposited by RF magnetron sputtering to improve adhesion, followed by Pt bottom electrode deposition.

A PZT precursor of morphotropical composition, Zr/Ti= 53/47, was made according to the modified 2-methoxyethanol route described by Gurkovich and Blum [4] and Budd et al. [2]. A similar precursor for $PbTiO_3$ was made with 30% Pb excess to enhance seed layer orientation and to avoid problems related to lead evaporation.

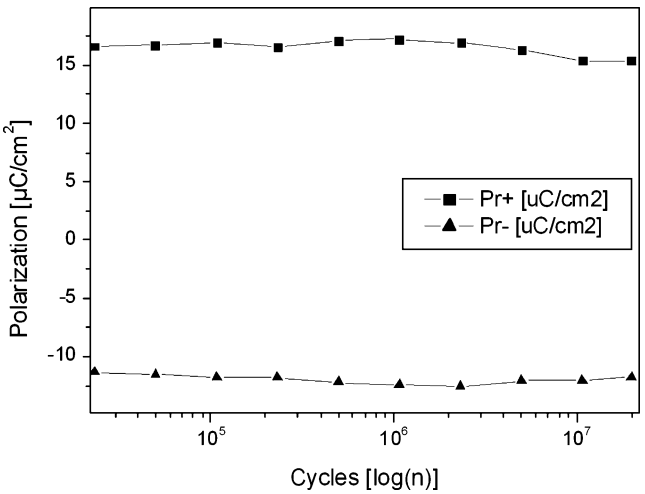

Fig. 7 Development of the remanent polarisation with the number of cycles during the fatigue test

A thin seed layer of $PbTiO_3$ was deposited using spin coating and subsequent pyrolysis as described in [11]. The purpose of the seed layer was to obtain {100} oriented PZT as this orientation has been reported to give the highest transverse piezoelectric coefficient, $e_{31,f}$ [6]. An approximately 2 µm PZT film was deposited on the seeded wafer using 32 sequential spin-on depositions and eight heat treatments at 650 °C according to a procedure already described in literature [6, 9]. This PZT thickness was chosen as an industrially relevant compromise between cost (limited number of depositions) and performance (sufficient layer thickness). Cr/Au top electrodes were deposited using vapour deposition and patterned by lift-off.

The PZT was patterned by etching in HCl/HF [12], and the backside cavity was opened by tetramethylammonium hydroxide (TMAH). The backside etch stopped at the buried oxide layer, which was then removed by HF. Finally, the cantilever was released by reactive ion etching.

2.3 Poling and testing

The wafer was mounted on a programmable xyz-table with a probe station and a heating chuck. The devices were addressed sequentially and poled at 150 °C/40 V for 10 min each. After cooling to 20 °C, C(V) curves were recorded from 0 to 20 V using an Agilent 4284 LCR meter with DC input. The measurements gave values for the dissipation factor (tanδ) directly, whereas the relative dielectric constant (ε_r) was calculated from the measured capacitance and the total area of the electrodes. Polarisation curves were recorded for selected cantilevers using a TF 2000 ferroelectric analyser (aixACCT Systems GmbH, Germany). Deflections of the cantilevers at zero field were recorded using white light interferometry (WYKO NY-2000, Veeco Instruments Inc., USA) [3].

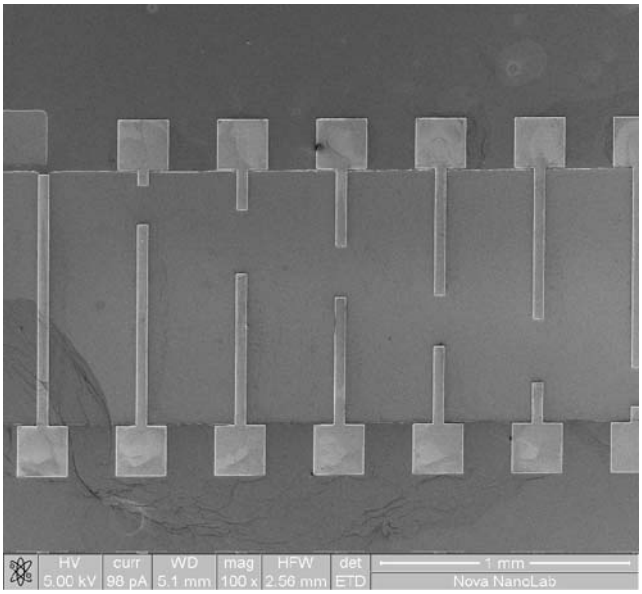

Fig. 8 SEM micrograph of cantilevers with various lengths, taken prior to release (micrograph by FEI Company, The Netherlands)

3 Results and discussion

3.1 Multimorph structure

A wafer that had been processed identically but not released was cut into thin sections using focused ion beam (FEI Company, The Netherlands). The SEM micrograph in Fig. 5 of one section shows the layers of the multimorph, including 8 layers in the PZT. The crack in the PZT layer that is visible to the right in the micrograph originates from an underlying crack in the SiO_2 layer. Otherwise, very few defects were observed.

3.2 Performance and uniformity across the wafer

The transverse piezoelectric charge coefficient $e_{31,f}$ was measured at 3 MPa applied tensile stress and frequencies between 0.1 and 10 Hz using a newly developed 4-point bending technique [8]. The measured values shown in Table 1 are even higher than previously reported data of similar films [6]. A review by Trolier-McKinstry and Muralt [10] reported the overall accepted value of $e_{31,f}$ for PZT thin films near the morphotropic phase boundary as -12 C/m^2 for (100) oriented films. Our experience is that the use of CSD seeding influences the transverse piezoelectric coefficient favourably compared previously sputtered seed layers.

Automated measurements of relative dielectric permittivity at 0 V and 1 kHz on more than 200 devices at various locations on the wafer surface showed that 98% were within ±16% of the average value (88% were within ±7%). Similar measurements of the dielectric dissipation factor showed that 99.5% were within ±34% of the average value (86% were within ±17%). The average values and standard deviations are shown in Table 2.

3.3 Fatigue test

A 5 kHz fatigue signal at ±25 V was applied to a typical cantilever. After 2×10^7 bipolar fatigue cycles, corresponding to 1 h continuous testing, less than 10% reduction of the remanent polarisation was observed, as shown in the hysteresis loops recorded before (Fig. 6a) and after (Fig. 6b) the fatigue test, respectively, and the development of the polarisation with number of cycles (Fig. 7). The asymmetry of the polarization loops can be ascribed to hot poling with +40 V. During hot poling, defects (typically oxygen vacancies) pin domains with polarization along the poling field. As a consequence, polarization reversal during loop measurement becomes incomplete, and the coercive fields become unequal. The low maximal field of 125 kV/cm is under these conditions insufficient to reach saturation polarization in the reversed direction. The fatigue test with switching can be considered as an accelerated test. Under normal operation of real devices much smaller voltage amplitudes will be used in reversed direction. Therefore, devices in operation will be even less prone to depolarisation.

3.4 Deflection of cantilevers

Figure 8 shows an array of 50 μm wide cantilevers of various lengths prior to release. The out-of-plane deflections of the same released structure are shown colour coded in Fig. 9, as measured by white light interferometry. The deflection of a typical long cantilever (800 μm) was 8.8 μm

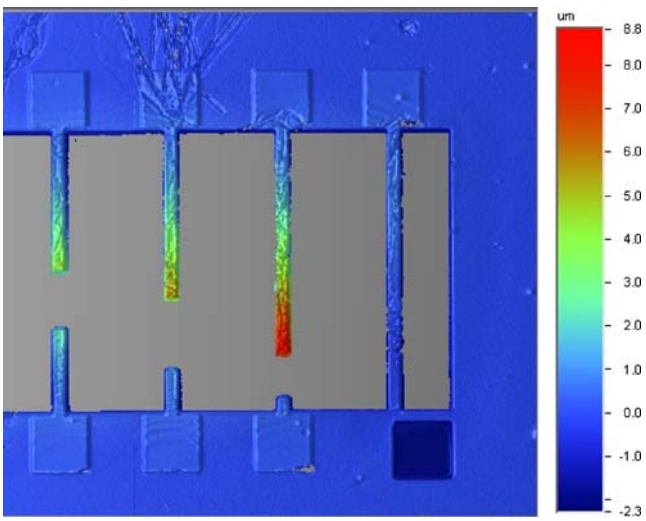

Fig. 9 Topography map of the same structure as the micrograph in Fig. 8, recorded by white light interferometry

out of the wafer plane, thus 1.1%. The measurements were made after poling of the devices.

4 Conclusions

Piezoelectric thin film elements are attractive as sensing and actuating elements in Si-based microsystems. In order to realise industrial production of piezo-MEMS, the performances obtained in research laboratories have to be reproduced under the conditions and scale of industrial production—with high yield, uniformity and reliability. Since hundreds of devices can be processed in parallel on each wafer, small-scale industrial production can be made in foundry laboratories using mostly existing equipment provided reliable industrial procedures are available.

This study has shown that a large number of working devices of different designs and sizes can be integrated on one wafer with a high degree of uniformity and good performance. More than 200 devices on one wafer have been poled and tested sequentially by an automatic system. Preparation techniques that have recently been developed in laboratories have been successfully implemented, including seeding to obtain the desired {001} PZT orientation, and adjusting the SiO_2 layer thickness to avoid deflection of the cantilevers. Fatigue tests have shown that cantilever oscillations with more than 10^7 cycles of ±25 V amplitude do not weaken the polarisation of the piezoelectric film significantly.

The present work is a part of an on-going project with the objective to develop reliable and qualified procedures for piezo-MEMS production at small scale. After completion of the wafer-level testing that is reported in this paper, the wafer was diced into 15×15 mm square samples and samples for 4-point bending tests. Results from testing of the diced samples and further results from the project will be reported in separate publications.

Acknowledgements The authors acknowledge the support from the European Commission through the MEMS-pie project (www.sintef.no/mems-pie) and contributions from the end-user companies involved: Hök Instrument AB (Sweden), Noliac A/S (Denmark), Precision Acoustics Ltd. (UK) and Sonitor AS (Norway).

References

1. W.E. Booij, A.H. Vogl, D.T. Wang, F. Tyholdt , N.P. Østbø, H. Ræder, K. Prume, J. Electroceramics, (2006) (in press)
2. K.D. Budd, S.K. Dey, D.A. Payne, Br. Ceram. Proc. **36**, 107 (1985)
3. P.J. Caber, Appl. Opt. **32**(19) 3438 (1993)
4. S.R. Gurkovich, J.B. Blum, in *Ultrastruct. Process. Ceram., Glasses, Compos*, ed. by L.L. Hench, D.R. Ulrich (Wiley, NY, 1984), p. 152
5. N. Ledermann, P. Muralt, J. Baborowski, M. Forster, J.-P. Pellaux, J. Micromechanics Microengineering, 1650 (2004)
6. N. Ledermann, P. Muralt, J. Baborowski, S. Gentil, K. Mukati, M. Cantoni, A. Seifert, N. Setter, Sens. Actuators, A **A105**, 162 (2003)
7. P. Muralt, J. Micromechanics Microengineering **10**(2), 136–146 (2000)
8. K. Prume, P. Muralt, F. Calame, T. Schmitz-Kempen, S. Tiedke, IEEE Trans. Ultrason. Ferroelectr. Freq. Control **54**, 8–14 (2007)
9. A. Seifert, N. Ledermann, S. Hiboux, J. Baborowski, P. Muralt, N. Setter, Integr. Ferroelectr. **35**, 159 (2001)
10. S. Trolier-McKinstry, P. Muralt, J. Electroceramics **12**, 7–17 (2004)
11. F. Tyholdt, F. Calame, K. Prume, W. Booij, H. Ræder, P. Muralt, J. Electroceramics, (2006) (in press)
12. L.P. Wang, R. Wolf, Q. Zhou, S. Trolier-McKinstry, R.J. Davis, Mater. Res. Soc. Symp. Proc. **657**, EE5 39/1 (2001)